Current Carrying Capacity of Vias

Some Conceptual Observations

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We are frequently asked about the current carrying capacity of vias. To our knowledge, there have been no studies of this particular topic, although we do know of people who have useful insights into this issue. What we offer here are some observations and a conceptual framework for looking at the issue, with some resulting guidelines that seem reasonable.

Background: When current flows along a trace, there is an i^2R (power) loss that results in localized heating. This causes the trace to increase in temperature. The trace cools by conduction into neighboring materials or convection into the environment. Stability, and therefore a stable temperature, is reached when the rate of heating equals the rate of cooling. We have previously reported on some studies of this effect[1], and UltraCAD has created a freeware calculator for predicting currents and temperatures.[2]

Trace heating is a function of cross sectional area. Trace cooling is a function of surface area and environment (such as external vs internal.) Perhaps these same fundamental principles can be applied to vias when looking at their current carrying capacities.

Consider **Figure 1**. The cross sectional area of the trace is found by multiplying its width (W1) by its thickness (T1). A via placed somewhere along the trace has a cylindrical geometry, with a finished diameter D2 and a wall thickness T2. Therefore, the outer diameter of the cylinder is D2+2*T2. The cross sectional area of the via's cylindrical structure is p times the average diameter (D2+T2) times its thickness, T2, or p*(D2+T2)*T2.
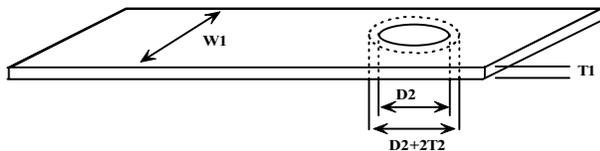
Figure 1: Relationship of a via to the trace it is placed in.

Via Fabrication: Vias are normally specified on the fabrication drawing by their inner "finished" diameter, D2, and wall thickness, T2. The fabricator drills a wide enough hole to accommodate the plated thickness of the wall. Plating is an inexact process, and small differences in via wall thickness may occur at different places on the board.

Normally, the final plating process, which defines the via wall thickness, also adds plating to all the other surface traces and pads on the board. If we are dealing with significant plating thicknesses, then allowance for this must be made in defining trace and pad separations and trace impedance calculations, etc. For this reason, designers are well advised to have the board fabricator on board early in the design process.

Equality: It seems reasonable that the current carrying capacity of the via is determined by the same thing that determines the current carrying capacity of the trace--cross sectional area and environment. Looking first at the cross sectional areas, they are equal for both the via and the trace when:

W1*T1 = p*(D2+T2)*T2

Using a little algebra, it can be shown that the cross sectional area of the trace and the cross sectional area of the via are equal when:

$$D2 = \frac{W1}{\pi} * \frac{T1}{T2} - T2 \qquad \text{(Equation 1)}$$

If we make the simplifying assumption that via wall thickness (T2) and trace thickness (T1) are the same (T), then equation 1 reduces to:

$$D2 = \frac{W1}{\pi} - T \qquad \text{(Equation 2)}$$

If we further recognize that T is usually small with respect to W1, then the *approximate* result is that the finished diameter of the via must be at least as large as the trace width divided by 3!

Cooling implications: It seems intuitive that a surface trace can cool more easily than an internal trace. A via connecting an external trace to an internal trace probably has an equivalent cooling capability between that of the two traces. Thus, using the dimensions of the internal trace would seem to be the conservative approach. If the via connects two

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internal traces, Equation 1 would seem to apply directly. On the other hand, if the via connects an external trace or connection to an internal plane, there is probably a sinking effect offered by that plane. In that case, one might speculate that a smaller amount of derating is necessary.

Solder coating: Solder coating has negligible impact on the current carrying capability of a trace. This is because the resistivity of solder as usually at least ten times (or more) that of copper. Therefore, even with a solder coat whose thickness is equal to the thickness of the underlying trace, over 90% of the current still flows through the copper. Similarly, a solder filled via will not increase the effective cross sectional area of the current path of the via. It may, however, increase the effectiveness of the conductive cooling of the via to the external surface. We know of no studies that have addressed this possibility.

Multiple vias: Designers and engineers frequently ask us if multiple vias are better than a single via. That is, for example, would five 8 mil vias be better than a single 40 mil via? **Figure 2** helps us see the (perhaps surprising) result. Vias contact traces or planes with a surface *area* defined by the outer circumference of the via cylinder and the thickness of the plane or trace (denoted as *a* in Figure 2.) This contact area is calculated as p*d*T. The transfer of heat between the via and the trace or plane would be directly proportional to this area.

Consider two vias, one with diameter d1 and the other with diameter d2. We can compare their contact areas as follows:

$$\frac{A1}{A2} = \frac{\pi * d1 * T}{\pi * d2 * T} = \frac{d1}{d2}$$

That is, the ratio of the contact areas is directly proportional to the ratio of the via outside diameters. The result is that n vias, of outside diameter d1 are equally effective as a single via whose outside diameter is n times d1, no more and no less. (Note: There are other cases where multiple vias are clearly better. For example, multiple vias can be effective in reducing overall via inductance and therefore increasing bandwidth. But these are different issues than the thermal issues being discussed in this article.)

It would be very beneficial for the industry if some resources were devoted to testing the conclusions drawn from these observations. Until then, these seem to be the most intuitive observations presently available to us all.
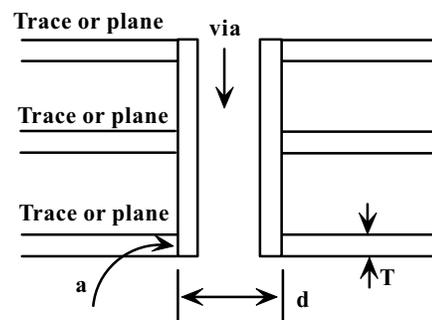
Figure 2: The contact area between a via and its connecting trace or plane is indicated by the arrow (a)

Footnotes:
1. "Trace Currents and Temperatures; How Hard Can We Drive 'Em?", May, 1998
2. UltraCAD's freeware Trace/Current calculator may be obtained at www.ultracad.com.

Note: Doug Brooks is President and Dave Graves is Vice President of UltraCAD Design, Inc Dave was a Top Gun winner at PCB West, 2001, and he has been designing circuit boards for as long as he can remember.