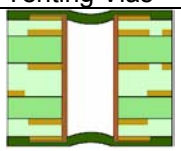
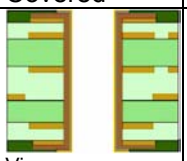
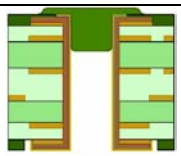
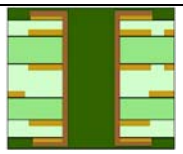
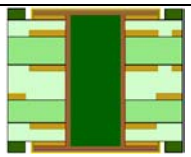
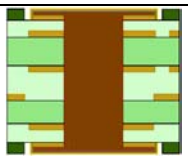
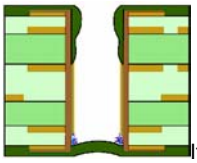
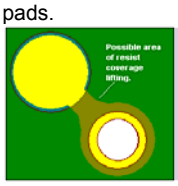
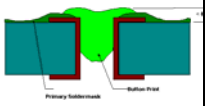
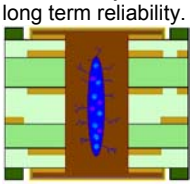
Purpose: The solder mask design, with respect to the vias, can dramatically effect the reliability and manufacturability of the PWBA. This document discusses the pros and cons of the various options.

Option	Primary LPI Solder Mask Tenting Vias	Vias Not Covered	Button Print	Plugged Via	Active Pad	Plating Vias Shut
Description	 No apertures are supplied on mask data layer. Mask covers via pads and tents hole. No surface finish is applied to via barrel. Possible entrapment.	 Vias are exposed. Surface finish is applied to via barrel.	 Vias tented one side by a secondary solder mask application. Surface finish is applied to via barrel prior to button print.	 Vias are plugged with mask or other non conductive media. LPI mask is applied over plug. No surface finish is applied to via barrel.	 Vias are plugged with a conductive or non-conductive media, planarized and plated over.	 Vias are specified to be plated shut with electrolytic copper.
History	In the past, tenting of vias with Dry Film Soldermask was standard offering. Due to the limitations on feature size resolution and high thickness for SMT applications of the Dry Film Masks, this process is not readily available. Assemblers may require plugged vias due to vacuum draw or to prevent paste wicking into vias.	Standard process.	This process was developed to allow a rework able, reliable via interconnect.	This process was developed as a modification from the LPI tent, but to guarantee that 100% of the vias are fully tented.	This process allows the use of via capture pads as SMT pads.	Old callout.
Pros	One step application.	Via barrels are covered with surface finish metal. Test access is available from both sides of card.	Via barrels are covered with surface finish metal. Test access is available from one side of card. Rework able as solder wicking is not a concern. Standard industry process.	100% of the required vias are tented.	Reduces routing issues on external layers. Minimizes inductance.	If feasible, a copper filled via increased thermal conductivity of the via.
Cons	Via tenting cannot be guaranteed with LPI mask. There are three common methods of applying LPI mask. Curtain, Spray and Screen coating. Curtain and Spray coating cannot ensure that the via is tented both sides. Screen coatings ability to tent is limited by the hole size, surface tension of the liquid mask, and board thickness.  If a via is not tented both sides, chemical entrapment from surface finish preclean lines is probable. All the finishes will be subject to a micro-etch process. The micro-etchant that gets trapped in the capped via will crystallize rapidly causing copper sulfate crystals. Over time, these crystals can cause long term reliability issues. In the case on ENIG finish, the gold and small area of exposed copper near the cap could form a galvanic cell, accelerating the etch process.	Possible wicking of solder paste into the via. In the case of BGA rework, paste loss due to wicking into the via is a result of the localized thermal energy causing the LPI mask to lift on the short distance between the ball and via capture pads.  This is not a concern at first pass assembly.	Perceived mask height issue at assembly. Industry max height of mask over copper has been reduced over the years from 0.004” down to 0.002”. Required an additional mask application process, post surface finish application. Not recommended for OSP or Tin finish. 	Additional process steps are required. No surface finish is applied to the via. Via size restrictive. Control of rate of rise during curing is critical to ensure 100% of volatiles are evacuated. Failure to control this can lead to soldermask smearing the surface during assembly reflow.	Multiple additional process steps are required, in addition to dual plating processes. The extra plating process has a negative effect on the minimum feature size capable on the external layers. This process is not advised in conjunction with PTFE substrates.	Reliability. Due to standard plating chemistries deposition in high throw areas at a greater rate than low throw areas (via barrel), the possibility of plugging the surface of the via prior to the center is extremely high. In this event, plating chemistries will be trapped in the via, and detrimentally effect the long term reliability.  The surface copper thickness will also be exceptionally high if a via could be reliably plated shut. This process is not advised until appropriate copper plating chemistries are developed specifically for plating shut through vias.

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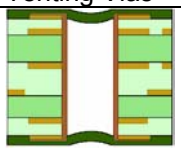
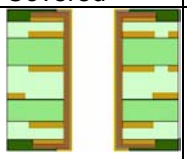
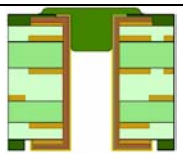
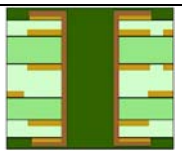
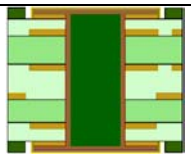
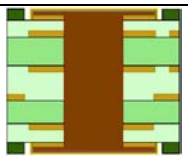
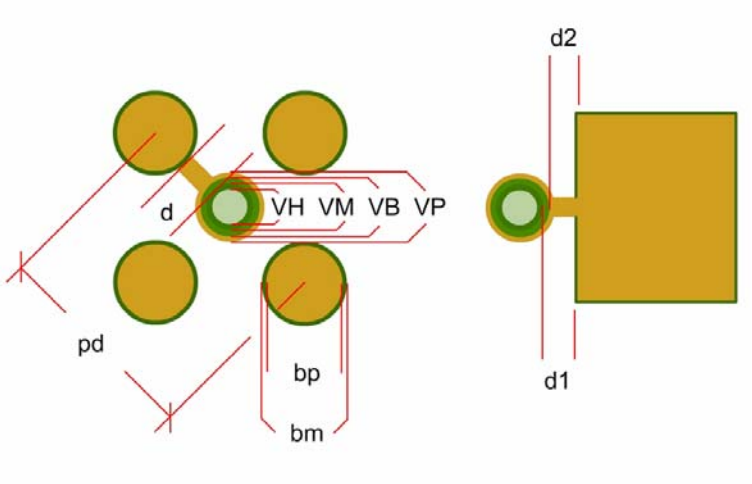
Description						
Cost Adder	No.	No.	No.	Minimal	High	N/A
Comment	NOT ADVISED for long term reliability. Many board designs are seen with vias tented via primary mask. This could be a result of a lack of reliability data.	ADVISED.	ADVISED.	Feasible	ADVISED for via in pad applications only.	NOT ADVISED



Feature	Symbol	1.27mm/50mils	1.00mm/0.3937mils	0.8mm/0.031496	Discrete
BGA Pad	bp	24	19	14	
BGA Mask (Cu defined)	bm	bp+5 (4 min)	bp+5 (4 min)	bp+5 (4 min)	pad+5 (4 min)
BGA Pad Dia. Dist.	pd	70.71	55.67	44.54	
Via Pad	VP	22-25	22	20	
Via Hole	VH	10-12	10	8-10	
Via Mask (Zit via)	VM	VH+5 (4 min)	VH+5 (4 min)	VH+5 (4 min)	
BGA Mask Dam	d	14.35-12.35 min	9.33-8.33	7.27-5.27	
Via Button Print	VB	VH+15 (10 min)	VH+15 (10 min)	VH+15 (10 min)	
Discrete Mask Dam	d1				4 min
Via Button to Pad	d2				10 min

** Based on 0.062 thick board, non solder mask defined bga pads and plastic bga packages. **
** Cu defined pad infers no mask will be present on the capture pad.**